

Systematic Optimization Methodology for mm-Wave Power Amplifiers

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Abstract—This paper introduces a systematic design optimization methodology for power amplifiers (PAs), emphasizing the role of electromagnetic (EM) simulations. A key aspect of the methodology is layout partitioning, which enables accurate full-structure modeling while optimizing computational efficiency. This partitioning approach facilitates high-accuracy EM simulations of the routing for electrically small elements, such as transistors and matching components. The influence of the ground plane on PA stability is examined, highlighting mechanisms that can lead to oscillations. Experimental validation using a test chip demonstrates the effectiveness of the proposed approach. Beyond power amplifiers, this methodology is broadly applicable to mm-wave circuit design, reducing both design iterations and fabrication effort for mm-wave circuit designers.

Keywords—power amplifier, electromagnetic modelling, electromagnetic analysis, millimeter-wave, stability.

I. INTRODUCTION

Introduction of 5G technology has transformed the way we communicate, pushing for faster, more efficient, and reliable wireless networks. Power amplifiers are essential part of 5G systems and play a key role in transmitting signals over various channels while maintaining signal quality and energy efficiency. Designing power amplifiers for 5G comes with new challenges, including the need for wider bandwidth, higher frequencies, better output power and efficiency. As 5G moves into millimeter-wave (mmWave) frequencies, accurate electromagnetic (EM) modeling has become more important than ever. Accurate EM modeling is especially critical for complex techniques like load modulation, envelope tracking, and Doherty amplifiers, which improve efficiency and signal quality. It also ensures that power amplifiers work effectively in advanced 5G systems like massive multiple-input multiple-output (MIMO) and beamforming. New tools that combine EM simulation with AI are making it easier to optimize designs and speed up development.

Multiple references are provided below, covering various design aspects and techniques related to power amplifier development. The operation of neutralization capacitors as well as bandwidth broadening technique with weakly coupled transformer is discussed in [1]. Also, voltage mode power combiner is presented in this paper. Broadband mm-wave PA is presented in [2], where all regular PA design aspects like biasing and load-pull are discussed. Dual band high gain PA is reported in [3]. Dual-band inter-stage matching network is discussed. [4] shows some aspects of EM modeling of passives standalone structures and their integration into simulation is also presented. Phase predistortion using varactors integrated in the input matching network for improving large signal

response is discussed in [5]. Reconfigurable PA deploying neutralization capacitors tuning is presented in [6]. The concept of adaptive feedback linearizers for improving output compression point i.e. both AM-AM and AM-PM responses, is presented in [7]. AI/ML based passive component synthesis are presented in [8] and [9].

The existing literature lacks a systematic methodology for power amplifier (PA) optimization using electromagnetic (EM) analysis. To address this gap, this paper presents a comprehensive mm-wave PA design approach that leverages fully EM-modeled test structures. Section II establishes the rationale behind the initial selection of PA component parameters and biasing conditions. Subsequently, the EM-based design flow is introduced to ensure accurate reproduction of measurement results. The discussion begins with top-level partitioning and optimal accuracy settings for the EM simulator. It then examines the influence of a non-ideal ground plane on PA stability, as well as the effects of internal inductors and baluns on S-parameters. Section IV presents and discusses the measurement results of the fabricated PA testchip. Section V concludes the paper.

II. INITIAL DESIGN FLOW

A. MOS Biasing

PA design starts with selection of the proper bias voltages for the MOS device which is normally N-type FET. For that purpose, NMOS performance characteristics are observed, i.e. transition frequency (f_t) and gain. The small signal gain is higher at lower gate-source biasing as the transistor is in weak inversion. On the other hand f_t increases at higher gate biasing voltage as it is directly proportional to MOS transconductance. To find a sweet spot figure of merit (FOM) function is derived, which is basically the product of those. As it can be seen

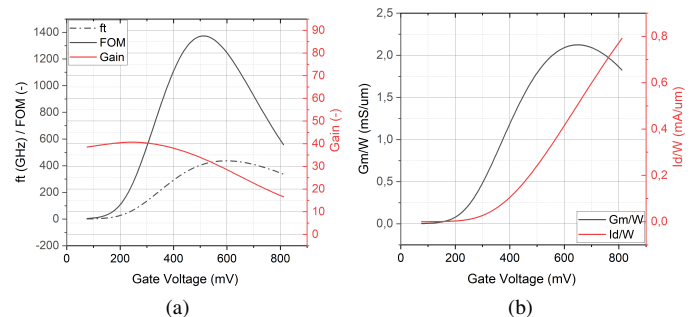


Fig. 1. NMOS Characterization Results: (a) Performance Curves; (b) Current Efficiency Curves

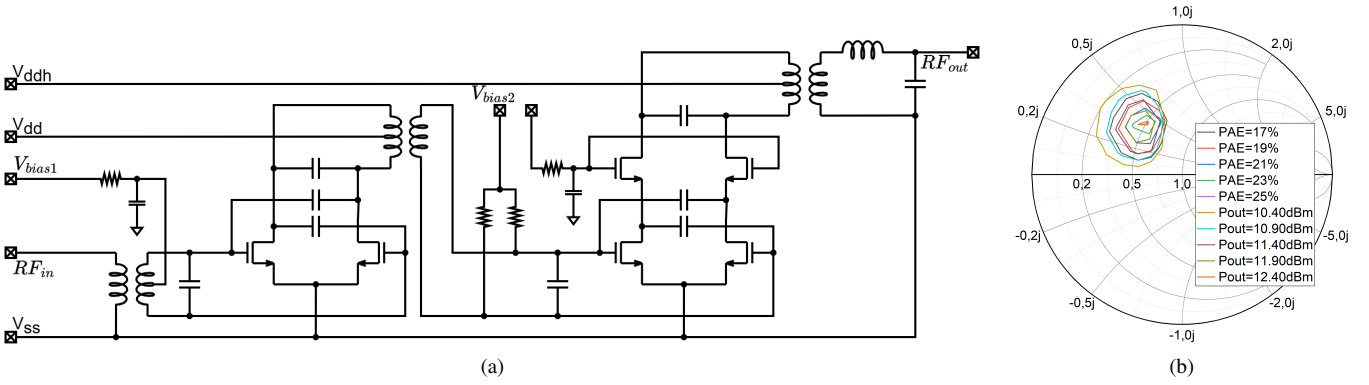


Fig. 2. Two Stage Power Amplifier: (a) Schematic Diagram; (b) Load-Pull Analysis of Output Stage

$V_{gs} = 500mV$ biasing give the best FOM value (Fig. 1a) [2]. However current efficiency metrics shall be also considered: although current efficiency (gm/W) increases with the gate biasing, simultaneously increasing nominal current per width creates problems with the local current density and hence heat dissipation. As a rule of thumb 50-70mV lower biasing is chosen, significantly decreasing current density (Fig. 1b), only marginally affecting FOM value. It is worth to mention that the biasing conditions do not depend on the actual width, as all the parameters, e.g. g_m , g_{ds} , C_{gs} scale with that.

B. Loadpull Simulations

After biasing has been chosen, device sizes have to be determined from the power to be delivered to the load.

$$P_{load,max} = (V_{o,max} - V_{d,sat})^2 / (2 \cdot R_{opt,load}) \quad (1)$$

$V_{o,max}$ is normally increased by adding cascode stages. Optimal load $R_{opt,load}$ is chosen accordingly to obtain the targeted delivered power and then transformed using the output matching network [1]. Fig. 2b shows the results of load-pull analysis of the output cascode stage. As it can be seen with the selected device size and biasing conditions, with the optimum load of $R_{opt,load} = 26 + j \cdot 40$, the $Psat=12.4$ dBm and $PAE_{max}=25\%$. This give some margin for the losses in the matching network. PAE calculations include the second stage so the expected value is reasonable.

C. Design

2-Stage 26 GHz PA design is illustrated in Fig. 2a. The target was to obtain 10 dBm output power, 24 dB small signal gain and 4 GHz 3-dB or 15 % fractional bandwidth. No linearizer had been implemented to avoid extra complexity in accurate correlation with the measurement results. Wideband inter-stage matching have been implemented. Cross-couple neutralization capacitors are optimized to increase the gain-bandwidth product under unconditionally stable operation. Also, second stage biasing resistors are used to flatten the frequency response. The cascode gates are properly tied to AC ground to decrease the feedback. Two stage matching network is implemented at the output to decrease the high quality factor caused by cascode output impedance.

III. EM DESIGN FLOW

To achieve accurate and reliable power amplifier designs, it is crucial to simulate the entire structure using an electromagnetic (EM) simulator, ensuring meticulous estimation of all significant parasitic elements. These parasitics, including capacitances, inductances, and coupling effects, can heavily impact performance, especially at high frequencies, making their precise evaluation essential for optimal design and layout. Many engineers focus on simulating individual components of a power amplifier separately, but they often overlook critical coupling effects between elements, which can significantly degrade performance, especially at high frequencies.

A. Partitioning

While simulating the entire test structure with high accuracy can be computationally intensive and require significant hardware resources, proper partitioning allows engineers to focus on areas that demand high precision while assuming minimal interaction with the rest of the electromagnetic structures. This approach balances computational efficiency with accuracy, enabling effective modeling of critical components without unnecessary resource expenditure. Fig. 3 shows the PA test-structure, where 2 PA stage cores have been removed from simulation setup to simulate separately. This testbench includes all access ports to the elements interacting with the ground plane: external excitation ports, decoupling capacitors access ports and interface ports to other partitions. As there are only thick metal available, it is possible to simulate with low accuracy the whole structure with a commercial EM simulator (e.g. EMX) in 2 hours, despite large amount of ports available. Without partitioning the simulation would run several days.

B. Transistors and Other Electrically Small Devices

While transistor models themselves are nowadays very accurate it is essential to model all the local routing to the ports defined in models. It is highly recommended to implement all the routing on higher layer thick metals without crossing device boundaries, as it ensures minimum impact on device model itself. However, sometimes it is not possible to reach all the ports, particularly for MOS devices. It is essential

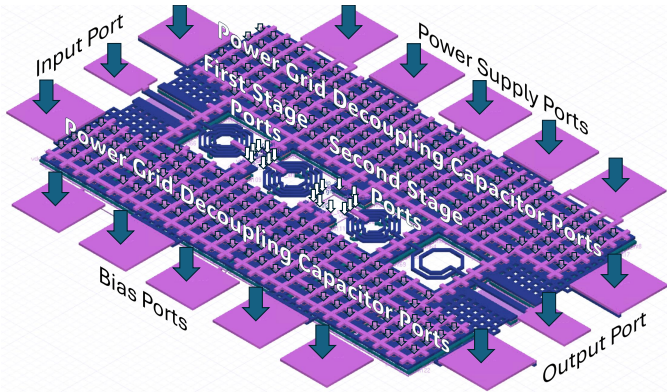


Fig. 3. HFSS View of the Ground Plane

to simulate the local routing with higher accuracy setting. It is recommended to partition individual stages, including all electrically small elements, e.g. transistors, matching capacitors and bias resistors, including local routing. It is valid to assume negligible interference with other passives, as the local routing doesn't have enough aperture to create any strong fields penetrating neighboring structures. Fig. 4a shows the simulation setup for the PA first stage, which includes the interface ports to the ground plane structure and device ports. Fig. 4b and 4c show zoomed in views of NMOS and capacitor devices routing. Devices are blurred as those are not part of the EM simulation. As it can be seen the gate connection is done using thin metal. For devices with many parallel transistors, if not accurately simulated, phase difference for the gate signals will not be properly modeled resulting in wrong (mostly false high) gain.

C. Parasitics and Harmful Interference in Ground Plane

Ground plane shall be kept reasonably far from baluns or inductors. However, often it is not possible because of several factors, e.g. necessity of certain decoupling capacitance, baluns and active stages need a proper ground, etc.

1) Unit Cell

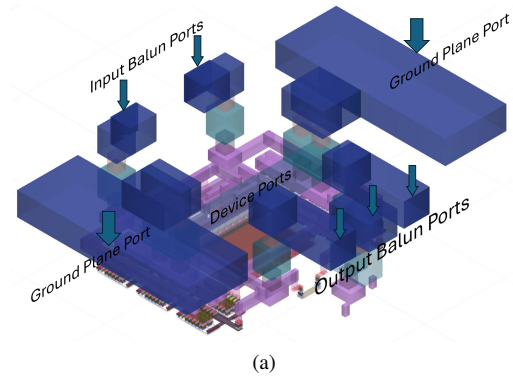
The decoupling capacitors are implemented mostly in a shape of unit cell (Fig. 3 right). Several factors shall be taken into account:

- ground plane cannot be solid not to violate the density rules, which results in a parasitic inductance
- this inductance appears in series with the decoupling capacitor. So, series self-resonance (SR) of the unit cell shall be near the operating band providing the low-ohmic bypass for the signals to be filtered

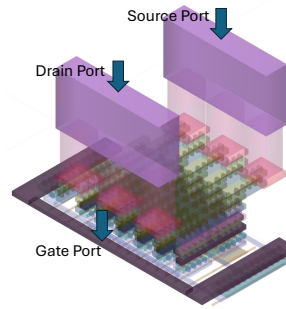
When the ground plane containing unit cell interacts with a nearby inductor, SR frequency changes according to Eq. 2, where Z_{ML} is the impedance seen by its edge interacting with the inductor.

$$F_{SR} = \frac{1}{\sqrt{2\pi \times C_{dec} \times \text{Im}(Z_{L_{par}} + Z_{ML})/\omega}} \quad (2)$$

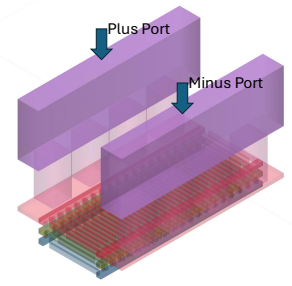
If the unit cell does not provide low-ohmic AC ground, longer current paths will arise, affecting the inductor performance.



(a)



(b)



(c)

Fig. 4. First stage EM setup views in HFSS: (a) First stage port locations; (b) NMOS port locations standalone; (c) APMOM port locations standalone

2) Interstage Feedback

Another issue can arise if decoupling capacitor doesn't provide a low ohmic AC ground, or there is no decoupling capacitor on ground pattern and there is no low-ohmic path to the ground pads. A signal path is formed, which provides a feedback between the stages potentially making the whole structure unstable. The issue is more severe at higher mm-wave band high gain amplifiers, as the parasitic inductors have more impedance enabling amplified signal leaking back to earlier stages.

3) Bias Tee

Bias tees are another source of potential oscillation. Although the decoupling capacitors shall filter the bias signal, those connected in series with ground plane parasitic inductance (Fig. 3 left). Because of low-ohmic series resonance

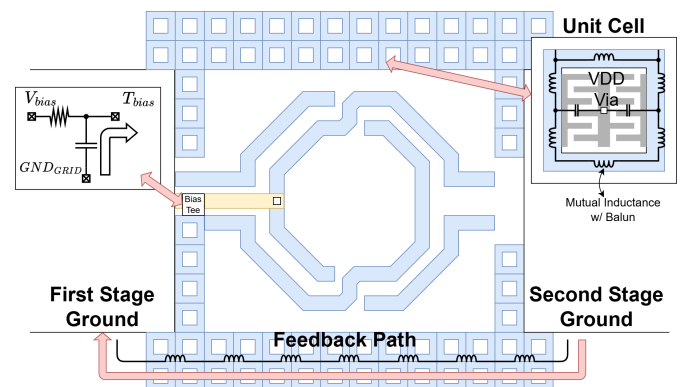


Fig. 5. Parasitic Interactions with Ground Plane

a negative impedance path can be created, where all the reverse common mode power is reflected back. This forms a reflection type oscillator structure and making PA unstable.

These effects cannot be observed without proper ground plane simulation. These concerns are even bigger at higher mm-wave bands and shall be mitigated at earlier design stages.

IV. MEASUREMENT RESULTS

Fig. 6 shows the PA die micrograph, which was implemented in 22-nm FDSOI process. S-Parameter measurements have been measured with Keysight N5224B VNA. As shown in Fig. 7, there is a strong correlation between the simulation and measurement results. The figure compares the measured data with two sets of simulation results. Both simulations account for ground plane parasitics; however, in one case, the inductors and baluns are simulated independently, without considering mutual coupling effects. As it can be observed, it results in significant shift in frequency for S_{11} . Also S_{21} peak frequency is shifted ~ 800 MHz lower and there is a ~ 1.5 dB deviation in peak value, when the mutual coupling effects are not considered.

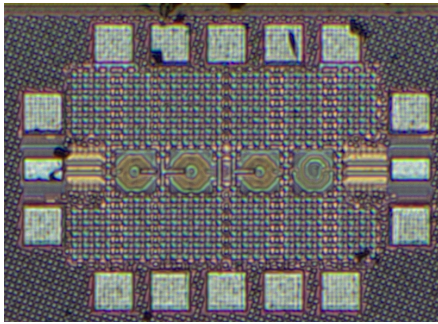


Fig. 6. Die Micrograph

V. CONCLUSION

The strong correlation between simulation and measurement results underscores the effectiveness of this methodology. By combining full-structure electromagnetic simulations, accurate estimation of parasitic effects, and strategic partitioning, it becomes possible to achieve high accuracy while optimizing computational resources. Additionally, this approach makes it easier to identify potential oscillations caused by ground plane or other parasitic coupling effects, ensuring greater stability and reliability in power amplifier designs for advanced mm-wave applications.

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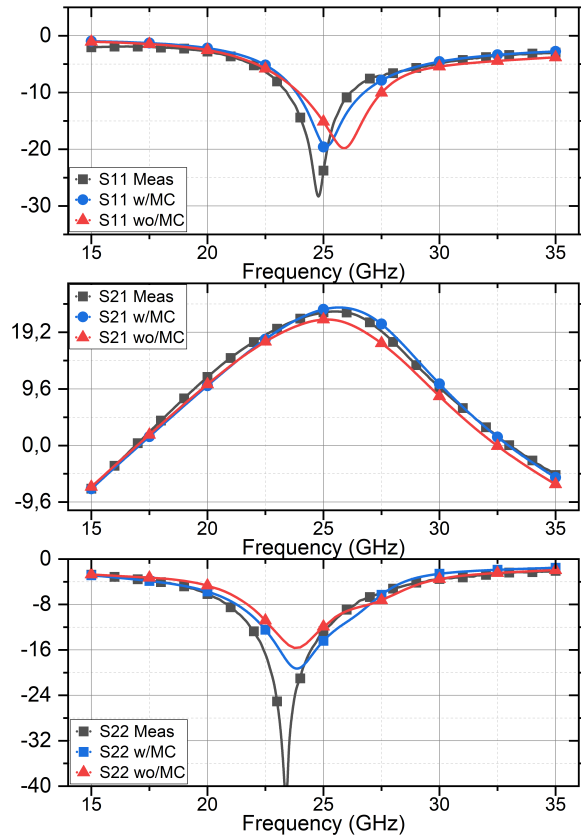


Fig. 7. Measured and simulated S-Parameters with and without mutual coupling

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