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A Compact Reconfigurable Power Splitter Enabling a Full-Duplex Integrated Transceiver Employed for Joint Communication and Radar Sensing

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***Abstract*— This paper introduces a reconfigurable power splitter that enables the implementation of a co-designed integrated front-end for Transceivers (TRx) towards Joint Communication and radar Sensing (JC&S) applications. Unlike the previous works, this work offers a flexible, compact, full-duplex, and fully-integrated solution in CMOS technologies with the help of a transformer-based power splitter, mm-wave switches, and digital control signals. For the proof of concept, the proposed reconfigurable power splitter is implemented on a silicon die in 22 nm FD-SOI technology within a compact core area of 0.1 mm^2. S-parameter measurements were carried out in K-band, the frequency range at which the power splitter is tuned. Finally, this work reports the achieved results in every possible mode of a JC&S system.**

***Keywords*— Joint Communication and Sensing, Transformer-based power splitter, 22 nm FD-SOI technology, K-Band.**

I. Introduction

Near future applications in 5G New Radio (NR) and 6G would provide ubiquitous communication in which tens of billions of devices connect to the wireless networks [1]. To enhance the power and performance optimization of these devices, it is essential to establish network synchronization and cooperative communications between the devices. For that, active and/or passive radar sensing can enable each communication device to provide a context-awareness of the environment in low power and privacy-friendly way [2]. This concept is called Joint Communication and Sensing (JC&S). Many autonomous objects such as vehicles, drones, etc. [3] can exploit JC&S to have efficient wireless communication. However, to deal with spectrum congestion, a device with JC&S capability should use the same frequency range for both communication and radar sensing [4][5]. Also, it is more power and area efficient to design a single hardware that works for both communication and radar sensing rather than dedicated hardware for each. Transceiver (TRx) architecture in both applications shares many blocks in the RF/mm-wave analog front-end (AFE). Hence, an energy-efficient solution for hardware implementation of JC&S seems feasible by employing co-designed TRx that can support both communication and radar sensing modes [6].

Fig. 1a shows an example of a wireless communication TRx front-end. For simplicity, direct conversion is assumed that is employed in many hardware implementations today. The direct conversion TRx comprises of low noise amplifier (LNA), power amplifier (PA), up-conversion and down conversion single side-band (SSB) mixer, variable gain amplifier (VGA), low pass filter (LPF), band pass filter (BPF), phase locked loop (PLL), digital to analog converter (DAC), analog to digital converter (ADC), and Rx/Tx digital signal processing (DSP). If the DSP supports matched filter analysis, the same analog front-end could also perform passive/active matched filter radar detection. This paper calls the analog front-end TRx in Fig. 1a as ”Mode1” that enables wireless communications as well as matched filter radar detection. While radar detection using traditional communication waveforms, e.g. orthogonal frequency division multiplexing (OFDM) can be implemented using matched-filter approach [2] but this architecture does not enable an efficient way to process traditional radar waveforms such as frequency modulated continuous waveform (FMCW). On the other hand, stretch processing radars such as ones using FMCW are commonly used and employed with a different front-end architecture shown in Fig. 1b. The received signal is mixed with a replica of the transmitted signal to generate the beat frequency. Further spectral analysis of a beat frequency by DSP estimates the range and velocity of an object. This front-end is called Mode2 used for stretch-processing radar detection.

A flexible JC&S system hardware should be able to support different use-case scenarios – radar centric or communication centric. Thus it needs to support different waveforms and signal processing architectures - a radar-centric energy-efficient analog processing (e.g. FMCW radar) and a communication-centric spectrally efficient digital processing (e.g. OFDM). Hence, both modes - Mode1 and Mode2 need to be supported. A co-existence approach uses both front-ends in Fig. 1 placed on the same board/chip. But, a co-designed method uses a single reconfigurable analog front-end to comply with communication and radar sensing applications. Hence, the signal processing in the digital domain has to support Mode1 and Mode2. In this way, power and area of the TRx are saved compared to the co-existence approach that employs two individual front-ends. Also, an efficient antenna reuse is only possible in co-design approaches.

Section II reviews the previous architectures for

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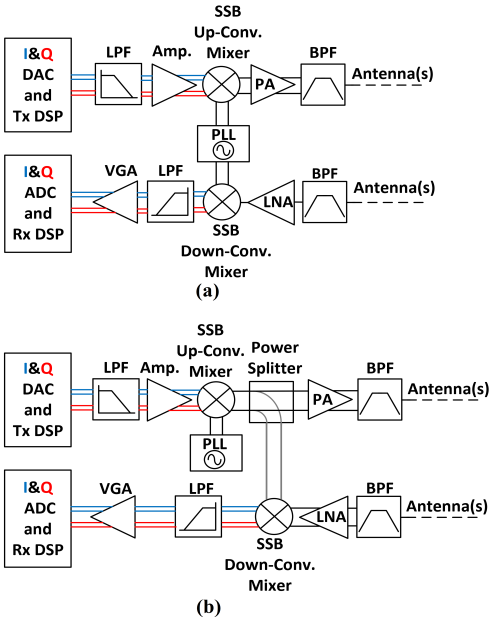

Fig. 1. Separate TRx front-end in (a) Mode1 and (b) Mode2.

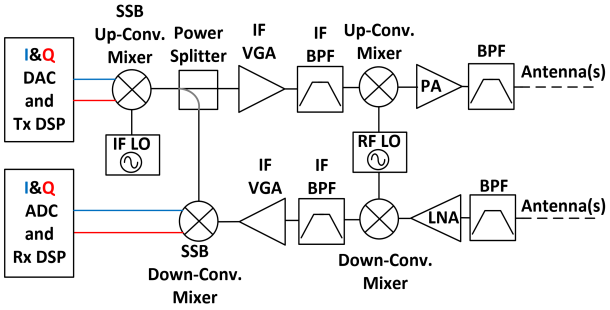

Fig. 2. JC&S front-end proposed in [8].

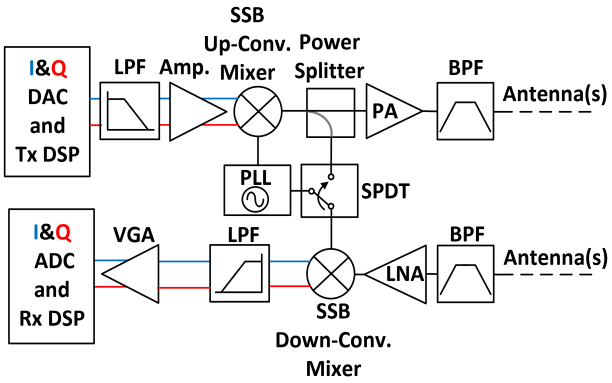

Fig. 3. A JC&S front-end similar to the one proposed in [10].

co-designed JC&S front-ends. Then, in section III, the proposed reconfigurable architecture for a JC&S front-end is introduced. Then, its working principles, as well as advantages over previous architecture, are explained. Section IV presents the measurement results and finally, section V draws conclusions.

II. Previously Reported Co-Designed JC&S Front-End

The JC&S front-ends reported in previous works, [7][8] are similar to the FMCW radar front-end in Fig. 1b. The communication link is realized with the same front-end thus limiting the usage to selected set of waveforms. The front-end proposed by [7] uses a direct digital synthesizer (DDS) to generate a chirp when it works in radar mode. In communication mode, the DDS works as a frequency shift keying (FSK) modulator to transmit/receive the signal. The front-end is implemented on an FR4 board with off-the-shelf components.

The work in [8] introduces a communication-radar modulation scheme, shown in Fig. 2, that operates in 5.9 GHz ISM-band. The JC&S front-end proposed in [9] employs the same architecture in 24 GHz ISM-band with a channel bandwidth of 250 MHz to achieve higher data rate in communication and range/velocity resolution in radar mode. In radar mode, the signal splits into two paths with an IF coupler implemented via Substrate Integrated Waveguide (SIW). In communication mode, the local oscillator (LO) at Rx must be unmodulated. On the other hand, baseband data modulates LO in Tx. Consequently, the Rx and Tx cannot work simultaneously and this TRx architecture can work only half-duplex when it is in communication mode.

The work in [10] proposed a full-duplex solution like the one shown in Fig. 3. The proposed front-end is compliant with both radar and communications by employing a Single Pole Double Through (SPDT) RF/mm-wave switch. During the communication (or passive radar) mode, Rx is separately fed by the fixed local oscillator (LO).

The drawbacks of the front-end architectures proposed so far are additional power loss in Tx communication mode for splitting the power. Secondly, power splitters are implemented via SIW coupler (shown in Fig. 2) or by integrated directional coupler (Fig. 3) that are bulky. Even implementing a directional coupler at RF/mm-wave frequencies (below 60GHz) is not an area-efficient power-splitting approach. The following section explains how this work addresses these issues by proposing a fully-integrated reconfigurable JC&S architecture in advanced node CMOS technology for the first time.

III. Proposed Reconfigurable Architecture

Fig. 4 presents the proposed reconfigurable JC&S architecture. It employs a compact transformer-based power splitter (T), high-frequency switches, and control bits (Φ_1, Φ_2). When Φ_1 = 1 (closed) & Φ_2 = 0 (open), as shown in Fig. 5a, the analog front-end operates in Mode1. At Tx, T acts as a power transformer between the up-converting Mixer and PA. In such a way, this structure avoids unnecessary power division, unlike the previous architectures. The PLL output goes to the down-converting mixer at the Rx so that the receiver can work independently. Therefore, another advantage of the proposed front-end is that it can work in full-duplex mode. When Φ_1 =

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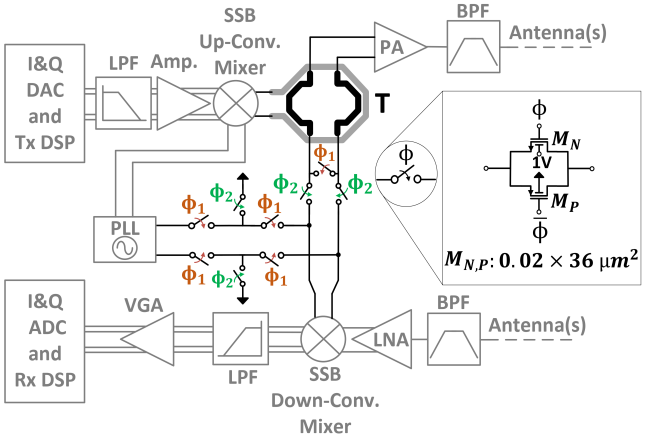
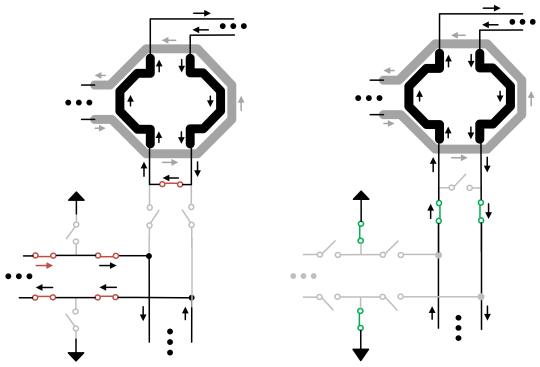


Fig. 4. Proposed reconfigurable JC&S front-end.



(a) (b)

Fig. 5. Proposed reconfigurable power splitter operation in (a) Mode1 and (b) Mode2.

0 (open) & Φ_2 = 1 (closed), T splits the power between Rx and Tx and configures the analog front-end to work in Mode2, as shown in Fig. 5b. The power splitter, T, is a two-turn spiral transformer that uses the top 4 metal layers. The switches are in a transmission gate configuration with the size of NMOS and PMOS in 22 nm FDSOI technology shown in Fig. 4. To further reduce the threshold voltage and the on-resistance values, the back-gate (available as an extra terminal in FD-SOI technology) of the NMOS and PMOS connects to VDD and GND, respectively. The switch sizes are selected such that their parasitic capacitance values would resonate with the inductive components of the splitter at the center frequency of interest, to reduce the power loss. Also, the Pi model switches in Fig. 4 improve the isolation between PLL and high-frequency signal path.

Breakthrough applications such as 5G, B5G, IoT, etc., can potentially operate in K-band utilizing already available 5G NR bands. This frequency range is a good option for a JC&S system since it provides a good amount of channel bandwidth to increase the data rate in communication and range resolution in radar mode. The implemented architecture is tuned to operate in K-band. The following section presents the measurement results in this band.

IV. Measurement Results

Fig. 6 shows the silicon implementation of the proposed reconfigurable power splitter in 22 nm FD-SOI technology from Global Foundries (22FDX). The core area of the implemented architecture (excluding the two output baluns at P2 and P4) is 0.1 mm^2. S-parameter measurement has been done to characterize the performance of the chip. Fig. 7 shows the setup for on-wafer measurements using RF and DC probes with 100 μm pitches. RF probe is a Z probe from Cascade in GSG configuration with 50Ω impedance. In Fig. 4, $Port_1$ (P1) represents the up-converting mixer output, $Port_2$ (P2) the PA input, $Port_3$ (P3) PLL output, and the input of the down-conversion mixer is named as $Port_4$ (P4). A 1:1 balun converts the differential quadrature outputs to single-ended and delivers it to the RF pads at P2 and P3. The capacitance at each pad is placed accordingly to tune the output in K-Band. These baluns are not part of the switch structure, hence, it is characterized separately and de-embedded from the output results shown later.

Rohde & Schwarz ZVA67 vector network analyzer is used for the S-parameter measurements. Fig. 8 shows the result of the proposed architecture when it is in Mode1. Based on the operation of the reconfigurable power splitter, the inputs are coming from P1 and P3. Hence S21 and S43 (same as S34) should peak at the frequency of interest and S41 and S23 should be quite low. The peak value of S21 is -3.7 dB at 22 GHz. The 3.7 dB loss in S21 includes the loss of access line from GSG pad to the input of T coil, loss of T coil, a switch, and balun with access line to GSG pad. Based on the EM simulations, the peak loss for the access line from GSG to the input of T and balun is 0.2 dB and 1.5 dB, respectively. Therefore, the combined loss should be excluded from the S21 since they are included only for measurement purposes and are not part of the main structure. -3 dB bandwidth (BW) falls within 16.5 GHz and 29 GHz. The peak value of S43 is -2.8 dB with -3 dB BW between 15.8 GHz and 33 GHz. Here the loss of the output balun at P4 is not part of the proposed structure. The peak value of S23 and S41 is less than -25 dB in the frequency range of interest which shows a low amount

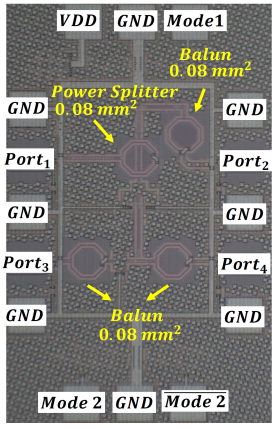


Fig. 6. Chip micro-photograph.

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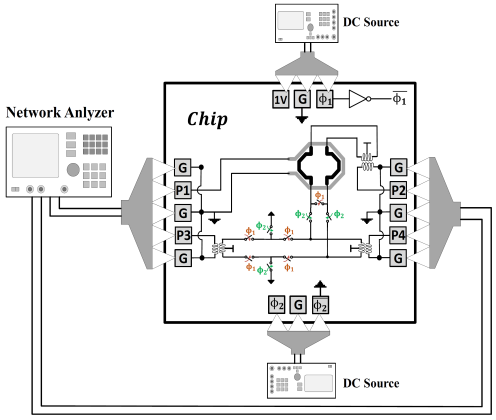

Fig. 7. Measurement Setup.

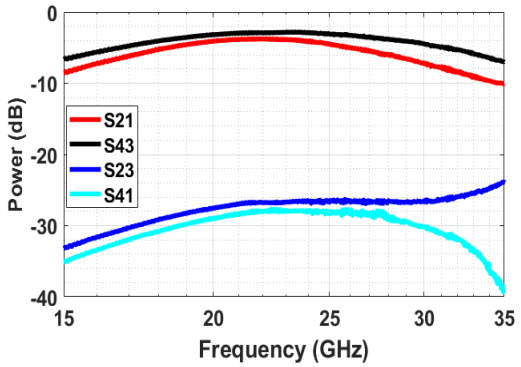

Fig. 8. Measured s-parameter of the proposed architecture when it is in Mode1 (ports shown in Fig. 7).

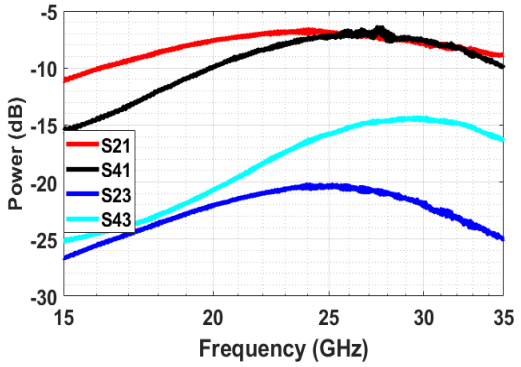

Fig. 9. Measured s-parameter of the proposed architecture when it is in Mode2 (ports shown in Fig. 7).

of PLL to transmitted signal leakage.

Fig. 9 shows the result when the proposed architecture operates in Mode2. The input signal coming from P1 should be split to P2 and P4 while P3 is isolated from both Rx and Tx. Therefore, S21 and S41 should peak at the frequency of interest and S43 and S23 should be quite low. The peak value of S21 is -6.6 dB at 24 GHz and S41 peaks at 27 GHz with value of -6.8 dB. The peak value of S23 and S41 is less than -14 dB in the whole frequency range of interest.

Table 1. Comparison of the proposed reconfigurable power splitter in JC&S front-end with previous works

	[7]	[9]	[10]	**This Work**
Center Frequency (GHz)	5.8	24	73.5	**22.5**
Full Duplex	No	No	Yes	**Yes**
CMOS integrated	No	No	N.A.	**Yes**
Tx excess loss in Comm.	Yes	Yes	Yes	**No**

V. CONCLUSION

For the first time, this work proposes a fully-integrated reconfigurable power splitter that enables a co-designed JC&S TRx front-end. Table. 1 summarized the advantages of the proposed reconfigurable power splitter over the ones in previously published JC&S front-end. By employing a compact transformer-based power splitter, digital control bits, and mm-wave switches, this work implements a full-duplex communication link without imposing excess loss in the Tx front-end. For the proof of concept, the reconfigurable splitter has been implemented in 22 nm FD-SOI technology. S-parameter results verify the peak performance for both communication and radar in K-band.

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