A 10.5 mW 60 GHz QVCO Employing Hybrid Back-Gate and Tail Inductive Coupling in 22 nm FD-SOI Technology

Farhad Bozorgi and Padmanava Sen, *Senior Member, IEEE,*

***Abstract*—This work introduces a Quadrature Voltage Controlled Oscillator (QVCO) that employs the proposed hybrid back-gate and tail inductive coupling technique. The implemented QVCO on silicon occupies a die area of 0.03 mm^2 in 22 nm FD-SOI technology. The power consumption of the QVCO operating with a 1 V supply voltage is 10.5 mW which, to the authors' best knowledge, is comparable to the state-of-the-art. The time and frequency domain measurement results in free-running mode show a Phase Noise (PN) of -112.1 dBc/Hz at 10 MHz offset from 60.2 GHz. The phase error throughout the whole tuning range is below 4.8 °. At 10 MHz offset, The QVCO in this work achieves FoM and FoM_A of -177.5 dBc/Hz and -192.7 dBc/Hz, respectively. They are in line among the bulk CMOS mm-wave QVCOs, despite the challenges imposed by short channel effects in 22 nm FD-SOI technology.**

***Index Terms*—22 nm FD-SOI technology, Quadrature Voltage Controlled Oscillator (QVCO), mm-wave, back-gate coupling, inductive coupling.**

I. Introduction

The growing demand for high-speed wireless video and audio data streaming in Augmented and Virtual Reality (AR/VR) applications has pushed 60 GHz wireless network protocols such as IEEE 802.11ad standard to be deployed in wireless transceivers (TRX) for such applications [1]. Additionally, near-future applications such as 6G and beyond may operate at D-band frequencies. Hence, the use of QVCO at 60 GHz along with frequency multipliers might be the solution to provide D-band LO. Another motive to design TRX at 60 GHz could be the short and mid-range communication and radar sensing in vehicular cruise control systems for greater precision and throughput without interference (due to additional atmospheric loss) [2].

Direct conversion Receivers (RX) and transmitters (TX) are well suited for fully-integrated solutions in which the compact area and low power consumption are the key benefits. Nonetheless, for a direct conversion TRX working at millimeter-wave frequencies, e.g., 60 GHz, the need for high-frequency quadrature Local Oscillator (LO) is a drawback. Quadrature LO generator is an essential block to enable higher-order modulation for increasing data throughput, image rejection [3], and phase shifting in phased array TRX [4].

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Farhad Bozorgi and Padmanava Sen are with Barkhausen Institut, Dresden, Germany (email:padmanava.sen@barkhauseninstitut.org).

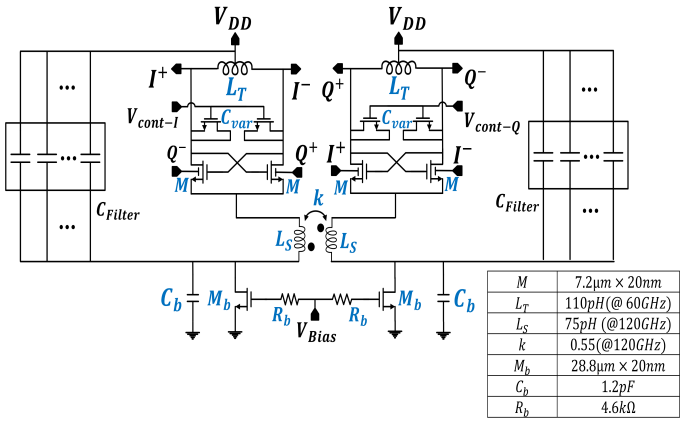
There are multiple techniques to generate the quadrature LO phases. Flip-flop based frequency dividers require at least twice the frequency at its input which may not be feasible for above 40 GHz applications. Hybrid couplers can equally split an input LO into two paths with a 90 ° phase shift between them. However, the inherent 3-dB loss and relatively large area make it less attractive for below 100 GHz integrated circuits. Poly-Phase Filters (PPF) employ lumped R-C branches to produce the quadrature phases. The low bandwidth and high phase error are the drawbacks that could be mitigated by cascading PPF stages at the cost of higher loss. Alternatively, Quadrature Voltage Controlled Oscillators (QVCO) use two coupled VCOs with differential outputs that can be implemented in mm-wave frequencies. The coupling could be through transistor pairs which impose additional PN. As an alternative to the traditional approach, this work exploits the idea of back-gate coupling. FD-SOI technology features the back-gate as an extra terminal that acts as a second gate. In addition to the active device coupling methods, capacitive or magnetic coupling could also be exploited. The latter is preferred since the on-chip transformers save the inductor area.

For QVCOs working at mm-wave frequencies, active gain and coupling factors could severely degrade due to parasitics. Consequently, locking might not happen and the PN would also get worse. Increasing the core power and/or employing additional coupling paths are possible solutions to overcome these issues. Due to these factors, designing mm-wave QVCO that is both power and area efficient would be challenging. This work combines active and passive coupling so that the two VCO cores would lock while minimizing the power and size. The QVCO has been implemented in 22nm FD-SOI technology. The power consumption of this work is state-of-the-art among bulk CMOS-based QVCOs. The three figures of merit for VCOs are FoM, FoM_T and FoM_A which are defined as:

$$FoM = PN@\Delta f - 10 * \log_{10}\left(\frac{{f_0}^2}{\Delta f^2} \cdot \frac{1mW}{P_{diss}}\right) \quad (1)$$

$$FoM_T = FoM@\Delta f - 10 * \log_{10}\left(TuningRange(\%)\right) \quad (2)$$

$$FoM_A = FoM@\Delta f - 10 * \log_{10}\left(\frac{1mm^2}{CoreArea}\right) \quad (3)$$



M	7.2μm × 20nm
L_T	110pH(@ 60GHz)
L_S	75pH (@120GHz)
k	0.55(@120GHz)
M_b	28.8μm × 20nm
C_b	1.2pF
R_b	4.6kΩ

Fig. 1: Proposed QVCO Circuit employing hybrid back-gate and tail inductive coupling technique.

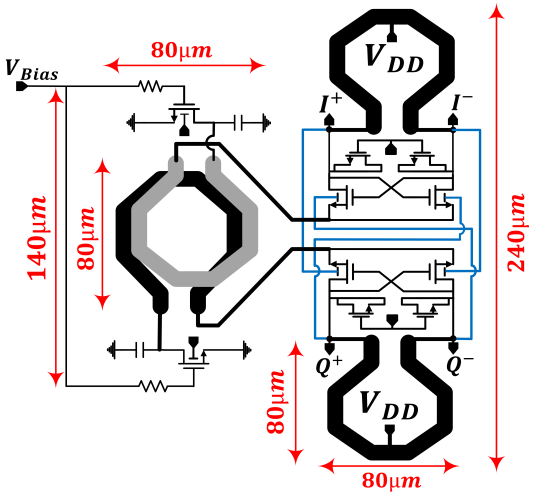


Fig. 2: Layout plan for the proposed QVCO.

For the proposed QVCO in FD-SOI, FOM, FOM_A and FOM_T are on par with those of the state-of-the-art bulk CMOS implementations.

Section II introduces the QVCO circuit design with the proposed method and explains its working principles. Section III presents the on-wafer measurement results of the implemented QVCO. Finally, section IV compares this work with some other mm-wave QVCOs and derives conclusions.

II. Proposed QVCO Circuit

Fig. 1 shows the proposed hybrid structure and associated design parameter values. First, the differential outputs of the two cores are directly connected to the back-gate of the cross-coupled pair to produce quadrature outputs. This is unlike the conventional approach where the anti-phase coupling is done between the two VCO cores with additional transistors and bias current sources which add extra noise to the output. The back-gate in FD-SOI technology has relatively lower junction capacitance which is advantageous since the back-gate capacitance is non-linear and may affect the output PN. In this design, the back-gate parasitic capacitance is half the front-gate capacitance. The two VCO cores are in a class-B mode where a tail current source (M_b) provides robust biasing. To avoid its flicker 1/f noise being up-converted to the output frequency, a relatively large capacitor (C_b) bypasses the output of the tail current source to the ac ground. In case of no coupling, the two VCO core would resonate at the frequency of the output tank which is $f_0 = \frac{1}{2\pi.\sqrt{L_T C_T}}$. C_T is comprised of N-type MOS varactor (C_{var}) controlled by an external voltage (V_{cont}) plus junction parasitic capacitance of the cross-coupled transistors (M). However, due to a back-gate coupling, there would be a shift to the center frequency where both cores resonate with 90° phase difference. This shift can be expressed as:

$$\Delta_f = \frac{f_0}{2Q_T} . tan^{-1} \frac{gm_{bg}}{gm} \tag{4}$$

Where gm and gm_{bg} are the gate and back-gate transconductance of the cross-coupled pairs, respectively, and Q_T is the output tank quality factor. The coupling factor can be derived as:

$$\alpha = \frac{gm_{bg}}{gm} \tag{5}$$

In this design, α is around 0.15 which is mostly dependent on the technology. This amount might not be enough to guarantee the locking in case of any mismatch between the two VCO cores. Based on the simulation results the minimum required value of α for this design is 0.22. Consequently, neither the quadrature phase nor good PN could be assured. To address this issue, the magnetic coupling between the tail of the two VCO [7] cores has been leveraged simultaneously. The transformer at the tail tries to ensure 180° out of phase at $2f_0$. Therefore, it provides an auxiliary tail inductive coupling path that helps to increase the overall α and ensure locking. Furthermore, this structure provides tail filtering. Since the cross-coupled transistors work in a hard switching mode, they enter the triode region. Because the output resonator sees a non-linear resistive path to the ground, its effective Q reduces. This issue is even worse at lower node CMOS technologies because of the short channel effects. With M_b shorted to the ac ground, a 75 pH inductor at the twice fundamental frequency at the tail provides a high impedance path to the ground and improves the PN. A distributed array of capacitances between VDD and GND (C_{Filter}) which AC shorts the VDD and GND with very low return path impedance.

The stand-alone magnetic coupling technique at mm-wave frequencies might not work. Because of the parasitics and inductor's Q degradation, the coupling coefficient between the two cores may be weakened. As a result, in this design, both back-gate and magnetic coupling techniques must be leveraged simultaneously to help each other to provide locking as well as improve the output PN.

Fig. 2 describes the layout plan of the proposed QVCO. The tail inductive coupling has been implemented using a 1:1 transformer. The inductive tanks for the oscillator core

outputs are realized by 1-turn spiral differential inductors with Q = 24 around 60 GHz. The routing lines for back-gate coupling between the two cores are matched in length to keep the symmetry and thus, avoiding the mismatch between the two cores. Additional layout measures are taken to minimize the asymmetry between the two cores. For example, a difference higher than 5 Ω for the line resistance between the cross lines of the two coupled cores would fail the quadrature lock in post-layout simulations. The bias current of the VCO cores could be tuned by V_{Bias} to counteract the process variation of the cross-coupled cores (gm_{bg}/gm) as well as transformers (k).

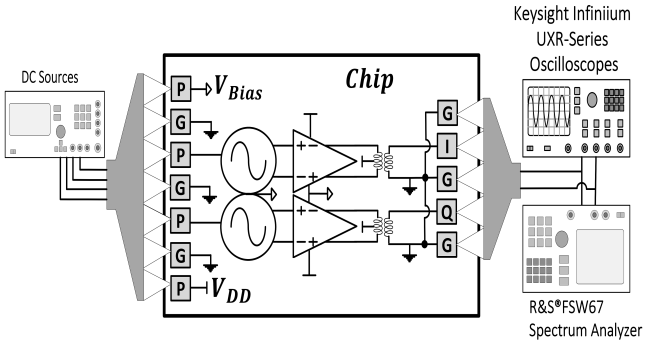


Fig. 4: Measurement Setup.

III. Measurement Results

Fig. 3 shows the silicon implementation of the proposed QVCO in 22 nm FD-SOI technology from Global Foundries (22FDX). The VCO core area is 0.03 mm^2. Fig. 4 shows the setup for on-wafer measurements by using RF and DC probes with 100 μm pitches. The QVCO core is followed by a wide-band buffer (employing inductive peaking) with a source follower output stage to drive the 50Ω load at each output. A 1:1 balun converts the differential quadrature outputs to single-ended and delivers it to the RF pads. RF probe is a Z probe from Cascade in GSGSG configuration.

Rohde & Schwarz FSW67 spectrum analyzer does the frequency and PN measurements. Based on the average measurement of four chips, the center frequency is 59.4 GHz with 3.2% Tuning Range (TR). Fig. 5 plots the output frequency versus V_{cont} for quadrature outputs. The values for V_{cont-I} and V_{cont-Q} are set equal.

Fig. 6 presents the measured PN while the QVCO is in free-running mode. When the spectrum analyzer locks to 60.2 GHz frequency, following the markers shows PN of −112.1 dBc/Hz at 10 MHz offset frequency. The measured $1/f^3$ corner frequency is 4 MHz. Also, the PN and corresponding FoM at 10 MHz offset frequency over the tuning range is shown in Fig. 7.

Keysight Infiniium UXR-Series Oscilloscope monitors the quadrature outputs in the real-time domain and measures the Phase Error (PE) and Amplitude Error (AE). As it can be seen from Fig. 8, at the center frequency of 59.4 GHz, the PE and AE is 0.8° and 0.9dB, respectively. The Phase Error throughout the whole range is less than 4.8 °.

The QVCO delivers −10 dBm power at the buffer output. The core consumes 10.5 mW from 1 V supply voltage. The power consumption of the buffer is 21 mW.

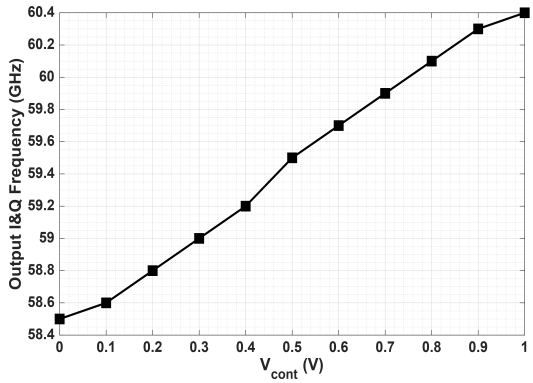


Fig. 5: Measured output frequency versus control voltage (V_{Cont}).

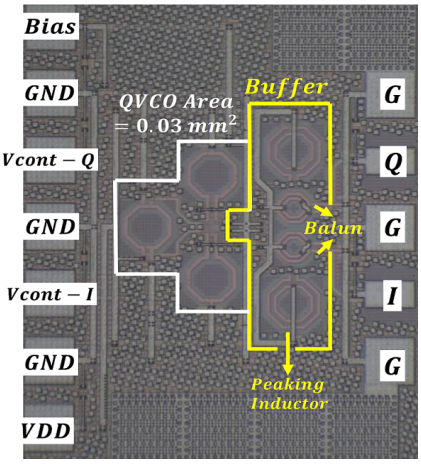


Fig. 3: Chip micro-photograph of the proposed QVCO core with output buffer and balun.

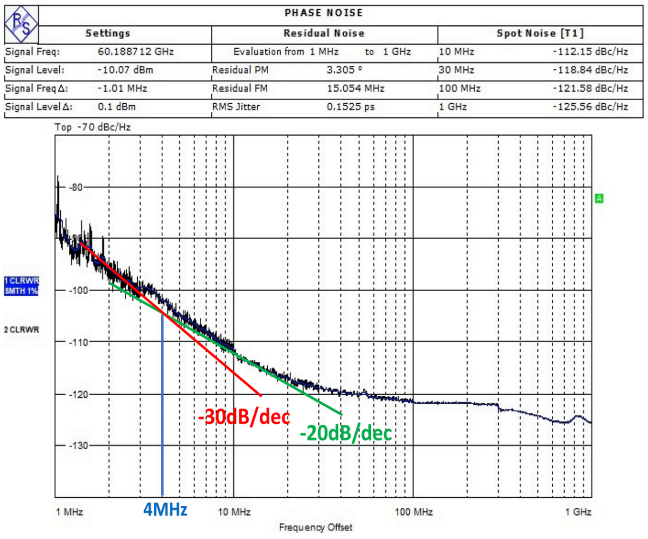


Fig. 6: Measured results for the PN vs. offset from 60.2 GHz.

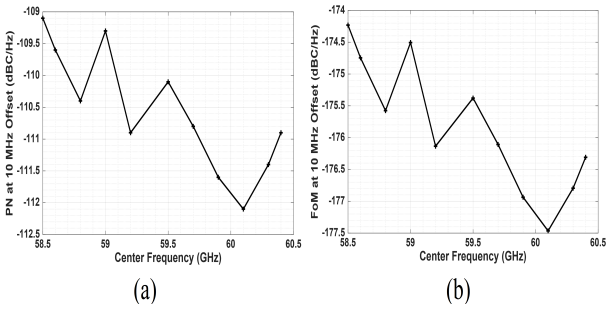


Fig. 7: Measured PN and corresponding FoM at 10 MHz offset frequency over the tuning range.

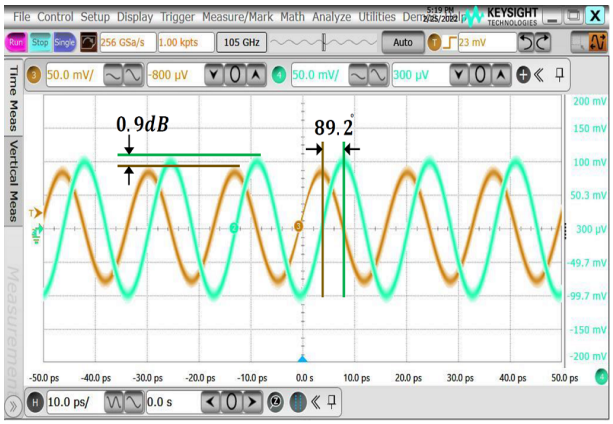


Fig. 8: Phase and Amplitude mismatch between I&Q output at 60.2GHz.

IV. Conclusion

This work introduced a 60 GHz QVCO with a proposed technique defined as hybrid back-gate and tail inductive coupling to provide locking between the two VCO cores with acceptable phase error. This methodology can extend the operating frequencies of reliable and low-power QVCO to E/F bands. Table I shows the performance comparison of this work with recently published mm-wave QVCOs. The power consumption of the QVCO in this work is state-of-the-art. Also, FoM, FoM_T and FoM_A (defined in Eq. 1, Eq. 2 and Eq. 3) are in-line with the other works in bulk CMOS despite the challenges imposed by short channel effects in 22 nm FD-SOI technology.

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TABLE I: Comparison with previously published mm-wave QVCOs in relatively low-node CMOS technologies.

	[8] EuMC '18	[9] TMTT '16	[10] TCAS-II '22	[11] ISSCC '14	**This Work**
Technology	FD-SOI 22nm	Bulk CMOS 28nm	Bulk CMOS 65nm	Bulk CMOS 40nm	**FD-SOI 22nm**
Supply Voltage (V)	0.8	1	1.2	0.9/1	**1**
Freq. (GHz)	61	72.7	28.97	62.6	**60.2**
Tuning Range (%)	16	6.4	18.1	16.2	**3.2**
Phase Error (°)	N.A	<1.5	<2	NA	**<4.8**
Power (mW)	51	35.6	<11	30	**10.5**
Phase Noise @10MHz (dBc/Hz)	-96[1]	-117.7	-118.7	-108[1]	**-112.1**
Core Area (mm^2)	0.02	0.03	0.06	0.16	**0.03**
FoM @10MHz (dBc/Hz)	-154.6	-179.4	-177.5>	-169.2	**-177.5**
FoM_T @10MHz (dBc/Hz)	-183	-187.5	-190>	-181.3	**-182.5**
FoM_A @10MHz (dBc/Hz)	-171.6	-194.6	-189.7	-177.1	**-192.7**

[1] Estimated from the curve

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